

Variable Reordering for Reversible Wave Cascades.

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Abstract—In this paper a theoretical background for the architecture of Reversible Wave Cascades is discussed, as well as some minimization algorithms for this architecture. Moreover, heuristic algorithms are proposed for estimating the optimal (or near optimal) variable ordering of a switching function, which drastically improves the simplification results of those, previously mentioned, algorithms. The topology of Reversible Wave Cascades is useful because it has been proved to be reversible and moreover it may help in the design of quantum circuits.

I. INTRODUCTION

Logic synthesis and its related problems of Boolean algebra constitute a hot scientific area and much research in this field has taken place over these last decades. For many years, logic synthesis was based on AND, OR and NOT gates. Recently the XOR (eXclusive OR) gate is being used in place of the OR gate, because it has been observed that it can reduce the complexity of most real-life application circuits [4].

A boolean (switching) function can be expressed in many different ways. Different expressions of a Boolean function may be useful in different situations e.g. implementing a function in a specific type of FPGA (Field Programmable Gate Array). Moreover it is usually desired to detect those expressions that are optimal, regarding a certain criterium, e.g. it may be desirable that the produced expression have the least possible number of variable literals. Finding suitable and optimal expressions for a Boolean function can be a very difficult and interesting mathematical problem.

In this work we deal with a special type of expressions called ESCT (Exclusive or Sum of Complex Terms) expressions. They can be mapped to a special cellular architecture called Reversible Wave Cascades (Fig. 1). It has been proved [5] that this special architecture can be directly mapped to reversible logic gates and more specifically to Generalized Toffoli gates. A logic gate is called reversible, if it has the same number of inputs, outputs, and maps each input vector into a unique output vector and vice versa. Moreover both fan-in and fan-out are forbidden. In [6] it has been proved that all quantum logic circuits must be reversible. Therefore ESCT expressions and the Reversible Wave Cascades architecture may aid in the designing of quantum circuits.

In order to form ESCT expressions for a Boolean function we may use the ESCT expressions of its subfunctions through relations known as Boolean decompositions. Ashenurst[1], Curtis[2], Roth and Carp[3] did pioneering work on the field of Boolean decomposition. An ESCT expression is a XOR sum of a special kind of terms, called complex terms.

This work has been funded by the project PENED 2003. This project is part of the OPERATIONAL PROGRAMME "COMPETITIVENESS" and is co-funded by the European Social Fund (75%) and National Resources (25%).

An arbitrary Boolean function has many ESCT expressions, having different numbers of complex terms. A minimal ESCT expression of a Boolean function is an ESCT expression with the least possible number of complex terms (this number is called the ESCT weight of the function). The ESCT weight of a Boolean function depends on its assumed input variable ordering. Therefore it is, usually, important to detect good variable orderings that allow us to produce ESCT expressions with the least possible number of complex terms.

In this work we present mathematical formulations that help us detect those ESCT expressions, of a certain Boolean function, that are minimal and even more we try to find appropriate variable orderings that produce the best possible results.

Some algorithms have been developed in the past, for mapping switching functions to cellular array architectures, similar to Reversible Wave Cascades, and then minimizing the number of the produced complex terms. In references [7], [8], [10], [11] techniques like variable reordering and cube transformation or even multi-valued logic are used, in an effort to minimize the number of complex terms, though their architectures differ from the one presented in this paper and are more complex. In references [12], [13] a systematic method was presented to produce architectures very similar to the Reversible Wave Cascade, by extending the EXORLINK [14] operation to complex terms. In Ref [5] an algorithm was proposed for mapping Reversible Wave Cascades to reversible gates (more specifically Generalized Toffoli gates), although it was not implemented. A similar reversible architecture is described in [15], with major objective to minimize the number of garbage inputs, although at that time no algorithm for the mapping and minimization of an arbitrary function to such architectures had been proposed. In Ref [9] BDDs (Binary Decision Diagrams) along with variable reordering techniques are used to produce cellular arrays. The architecture produced is similar to the Reversible Wave Cascades, although the output of each cell may be connected not only to its physical next but to others as well. In Ref [16] two algorithms were presented that produced ESCT expressions for a single-output boolean function while minimizing the number of terms in the produced expression. The first one guarantees minimality for functions up to 5 variables, while the second algorithm applied the first one on groups of cascades, inside the expression, as a term transformation operation. These algorithms have been improved in [17] with the introduction of relative terms and in [18] they have been extended for multi-output boolean functions. In Ref [19] a new algorithm is proposed which can detect minimal ESCT expressions for single-output switching functions of up to 6 input variables.

In this paper we give a brief description of the algorithms

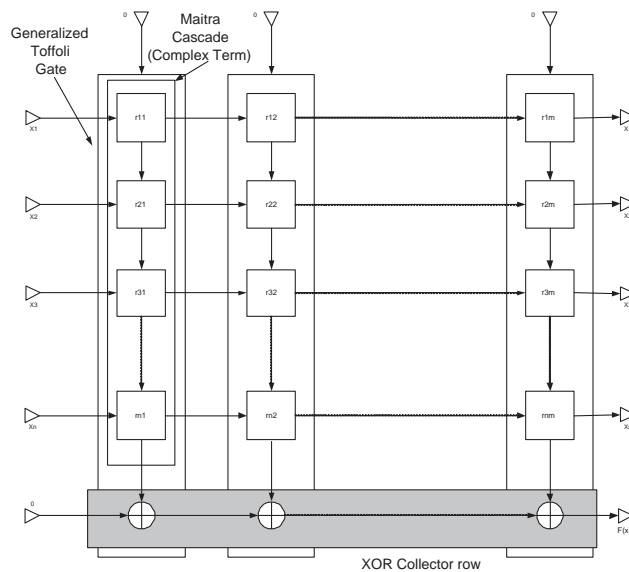


Fig. 1. Reversible wave cascade CA

presented in [16][17][18] and [19]. Moreover, some algorithms are proposed for the variable reordering problem, which can drastically improve the results of these previously mentioned minimization algorithms.

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